## AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Please cancel claims 2 and 5 without prejudice and amend claims 1 and 4 as follows:

## LISTING OF CLAIMS:

1. (Currently Amended) A modulator using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of a digital input signal from each other, wherein said component separating unit includes a first quantizer quantizing the digital input signal, and an adder adding said digital input signal to said signal component provided from said first quantizer;

single-stage delta-sigma modulator modulating the error component separated by said component separating unit; [[and]]

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said single-stage delta-sigma modulator; and

an attenuator connected between said adder and said single-stage delta-sigma modulator, and having a coefficient smaller than one,

wherein said single-stage delta-sigma modulator includes:

a plurality of integrators,

a quantizer quantizing an output of an integrator in a final stage, and

a delay element delaying an output of said quantizer to perform negative feedback by sending the delayed output to said plurality of integrators.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The modulator according to claim [[2]]1, wherein said single-stage delta-sigma modulator includes a plurality of single-stage delta-sigma modulators and

said plurality of single-stage delta-sigma modulators are cascaded.

5. (Canceled)

6. (Currently Amended) A modulator using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of a digital input signal from each other;

single-stage delta-sigma modulator modulating the error component separated by said component separating unit; and

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said single-stage delta-sigma modulator, wherein

said component separating unit includes:

a multibit quantizer quantizing the digital input signal to provide a multibit form, and

an adder adding said digital input signal to said signal component provided from said multibit quantizer.

7. (Canceled)

8. (Previously Presented) A modulator using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of an analog input signal from each other;

delta-sigma modulator modulating the error component separated by said component separating unit; and

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said delta-sigma modulator, wherein

said component separating unit includes:

a first quantizer quantizing the analog input signal,

a first digital-to-analog converter converting said signal component provided from said first quantizer to a first analog signal, and

an adder adding said analog input signal to said first analog signal provided from said first digital-to-analog converter,

wherein

said delta-sigma modulator includes:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage,

a second digital-to-analog converter converting an output of said second quantizer to a second analog signal, and

a delay element delaying the second analog signal provided from said second digital-to-analog converter, and performing negative feedback by sending the delayed analog signal to said plurality of integrators.

9. (Previously Presented) A modulator using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of an input signal from each other;

delta-sigma modulator modulating the error component separated by said component separating unit; and

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said delta-sigma modulator, wherein

said component separating unit includes:

a first quantizer quantizing an analog input signal,

a first digital-to-analog converter converting said signal component provided from said first quantizer to an analog signal, and

an adder adding said analog input signal to said analog signal provided from said first digital-to-analog converter, wherein

said delta-sigma modulator includes a plurality of single-stage delta-sigma modulators each including:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage,

a second digital-to-analog converter converting an output of said second quantizer to an analog signal, and

a delay element delaying the analog signal provided from said second digital-to-analog converter, and performing negative feedback by sending the delayed analog signal to said plurality of integrators; and

said plurality of single-stage delta-sigma modulators are cascaded.

10. (Previously Presented) The modulator according to claim 8, further comprising:

an attenuator connected between said adder and said delta-sigma modulator, and having a coefficient smaller than one.

11. (Previously Presented) A modulator, using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of an analog input signal from each other;

delta-sigma modulator modulating the error component separated by said component separating unit; and

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said delta-sigma modulator, wherein

said component separating unit includes:

a multibit quantizer quantizing the analog input signal to provide a multibit form,

a digital-to-analog converter converting said signal component provided from said multibit quantizer to an analog signal, and

an adder adding said analog input signal to the analog signal provided from said digital-to-analog converter.

12. (Previously Presented) The modulator according to claim 9, further comprising:

an attenuator connected between said adder and said delta-sigma modulator, and having a coefficient smaller than one.